SNx4HC10 Triple 3-Input NAND Gates

1 Features

- Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Wide operating temperature range: –40°C to +85°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

2 Applications

- Alarm / tamper detect circuit
- S-R latch

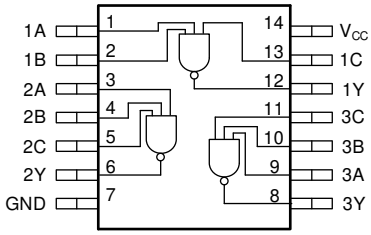
3 Description

This device contains three independent 3-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC10D	SOIC (14)	8.70 mm × 3.90 mm
SN74HC10N	PDIP (14)	19.30 mm × 6.40 mm
SN74HC10NS	SO (14)	10.20 mm × 5.30 mm
SN74HC10PW	TSSOP (14)	5.00 mm × 4.40 mm
SN54HC10J	CDIP (14)	21.30 mm × 7.60 mm
SN54HC10FK	LCCC (20)	8.90 mm × 8.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional pinout

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2003) to Revision E (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated to new data sheet standards	1
• $R_{\theta JA}$ increased for the D, DB, and PW packages and decreased for the N and NS packages	4

5 Pin Configuration and Functions

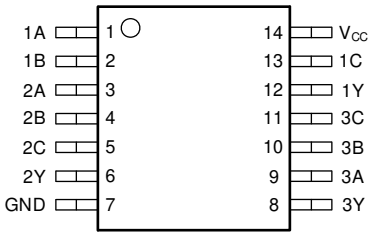


Figure 5-1. D, N, NS, PW, or J Package 14-Pin SOIC, PDIP, SO, TSSOP, or CDIP Top View

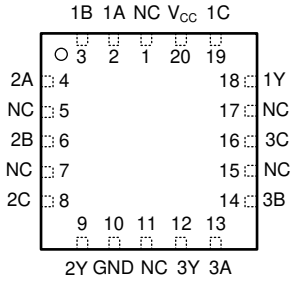


Figure 5-2. FK Package 20-Pin LCCC Top View

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, N, NS, PW, or J	FK		
1A	1	2	Input	Channel 1, Input A
1B	2	3	Input	Channel 1, Input B
2A	3	4	Input	Channel 2, Input A
2B	4	6	Input	Channel 2, Input B
2C	5	8	Input	Channel 2, Input C
2Y	6	9	Output	Channel 2, Output Y
GND	7	10	—	Ground
3Y	8	12	Output	Channel 3, Output Y
3A	9	13	Input	Channel 3, Input A
3B	10	14	Input	Channel 3, Input B
3C	11	16	Input	Channel 3, Input C
1Y	12	18	Output	Channel 1, Output Y
1C	13	19	Input	Channel 1, Input C
V_{CC}	14	20	—	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC10	–55		125	°C
		SN74HC10	–40		85	

6.3 Thermal Information

THERMAL METRIC(1)		SN74HC10					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6		67.5	122.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.0		55.6	81.8	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5		47.2	83.8	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5		35.6	45.4	25.2	°C/W

THERMAL METRIC(1)		SN74HC10					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	89.1		47.0	83.4	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics - 74

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			-40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V	1.9	1.998		1.9			V
				4.5 V	4.4	4.499		4.4			
				6 V	5.9	5.999		5.9			
			I_{OH} = -4 mA	4.5 V	3.98	4.3		3.84			
			I_{OH} = -5.2 mA	6 V	5.48	5.8		5.34			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1			0.1	V
				4.5 V		0.001	0.1			0.1	
			I_{OL} = 20 µA	6 V		0.001	0.1			0.1	
			I_{OL} = 4 mA	4.5 V		0.17	0.26			0.33	
			I_{OL} = 5.2 mA	6 V		0.15	0.26			0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V			±0.1			±1	µA
I_{CC}	Supply current	V_I = V_{CC} or 0	V_I = V_{CC} or 0	6 V			2			20	µA
C_i	Input capacitance			2 V to 6 V		3	10			10	pF

6.5 Electrical Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9			1.9			V
				4.5 V	4.4	4.499		4.4			4.4			
				6 V	5.9	5.999		5.9			5.9			
			I_{OH} = –4 mA	4.5 V	3.98	4.3								
			I_{OH} = –5.2 mA	6 V	5.48	5.8								
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1			0.1			0.1	V
				4.5 V		0.001	0.1			0.1			0.1	
				6 V		0.001	0.1			0.1			0.1	
			I_{OL} = 4 mA	4.5 V		0.17	0.26			0.33			0.4	
			I_{OL} = 5.2 mA	6 V		0.15	0.26			0.33			0.4	

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6 V			±0.1			±1			±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V			2			20			40	µA
C_i	Input capacitance			2 V to 6 V		3	10			10			10	pF

6.6 Switching Characteristics - 74

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A, B, or C	Y	2 V		35	95			120	ns
				4.5 V		10	19			24	
				6 V		9	16			20	
t_t	Transition-time		Y	2 V		23	75			95	ns
				4.5 V		6	15			19	
				6 V		5	13			16	

6.7 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A , B, or C	Y	2 V		35	95			120			145	ns
				4.5 V		10	19			24			29	
				6 V		9	16			20			25	
t_t	Transition-time		Y	2 V		23	75			95			110	ns
				4.5 V		6	15			19			22	
				6 V		5	13			16			19	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		25		pF

6.9 Typical Characteristics

T_A = 25°C

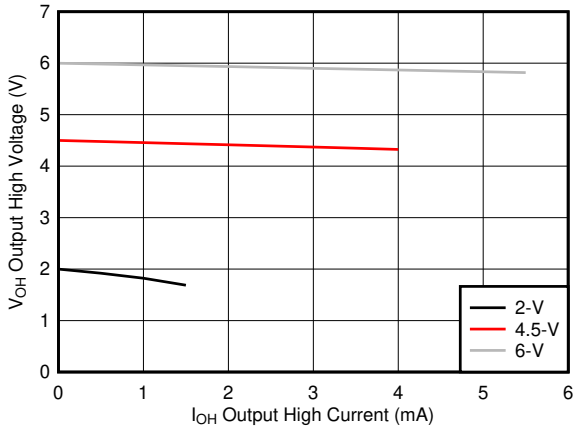


Figure 6-1. Typical output voltage in the high state (V_{OH})

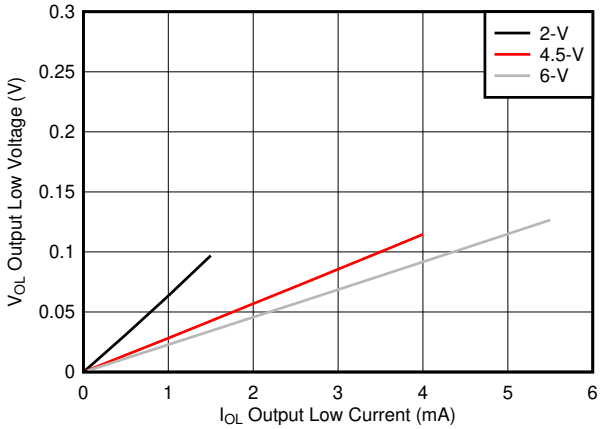
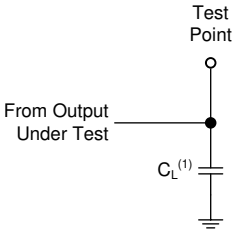


Figure 6-2. Typical output voltage in the low state (V_{OL})

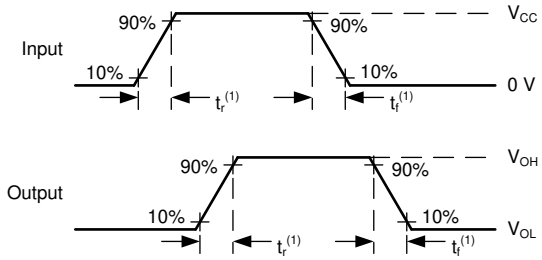
7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



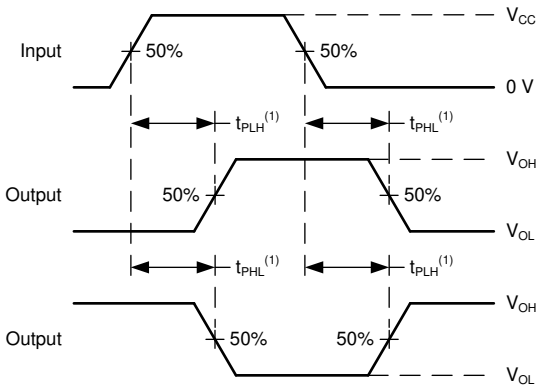
A. C_L = 50 pF and includes probe and jig capacitance.

Figure 7-1. Load Circuit



A. t_t is the greater of t_r and t_f.

Figure 7-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd}.

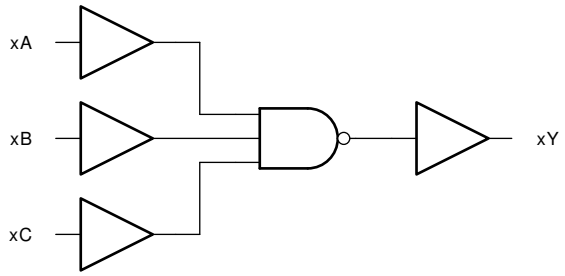
Figure 7-3. Voltage Waveforms Propagation Delays

8 Detailed Description

8.1 Overview

This device contains three independent 3-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C}$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC10 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics - 74* connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics - 74*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics - 74*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 8-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

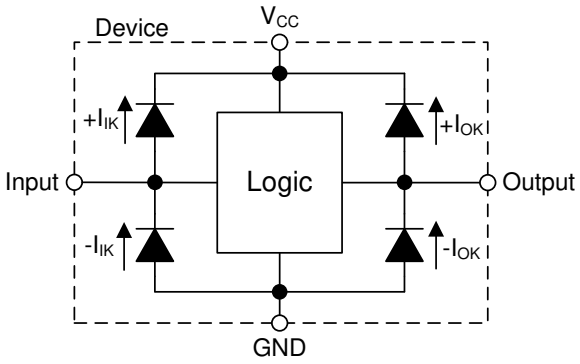


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, two 3-input NAND gates are used to create an active-low SR latch as shown in *Figure 9-1*. The additional gate can be used for another application, or the inputs can be grounded and the channel left unused.

This device is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

9.2 Typical Application

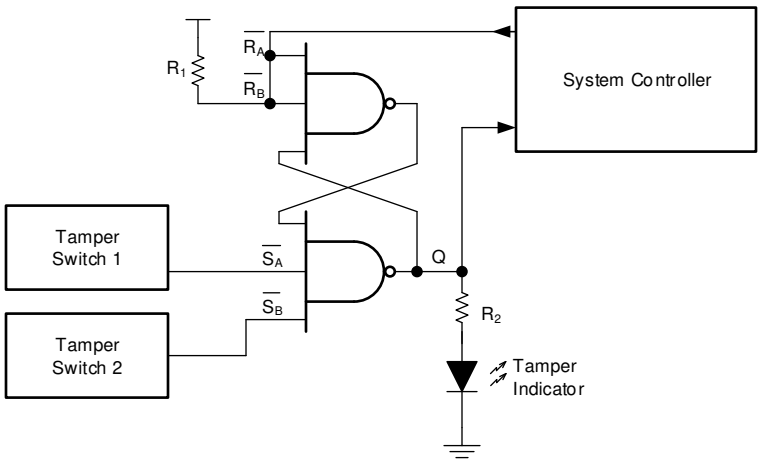


Figure 9-1. Typical application schematic

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics - 74*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC10 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics - 74*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC10, as specified in the *Electrical Characteristics - 74*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HC10 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to *Section 8.3* for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics - 74*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics - 74*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Section 8.3* for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in *Section 11*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC10 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

9.2.3 Application Curves

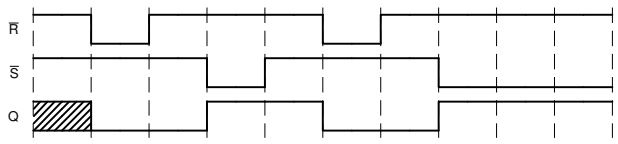


Figure 9-2. Typical application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 11-1*.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

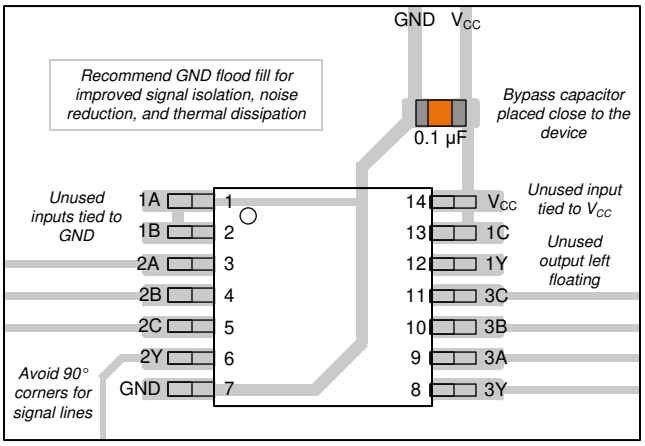


Figure 11-1. Example layout for the SN74HC10

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8403801VCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8403801VC A SNV54HC10J	Samples
84038012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84038012A SNJ54HC 10FK	Samples
8403801CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403801CA SNJ54HC10J	Samples
8403801DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403801DA SNJ54HC10W	Samples
JM38510/65002B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65002B2A	Samples
JM38510/65002BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65002BCA	Samples
M38510/65002B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65002B2A	Samples
M38510/65002BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65002BCA	Samples
SN54HC10J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC10J	Samples
SN74HC10D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10DT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC10N	Samples
SN74HC10NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC10N	Samples
SN74HC10NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC10PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SN74HC10PWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC10	Samples
SNJ54HC10FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84038012A SNJ54HC 10FK	Samples
SNJ54HC10J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403801CA SNJ54HC10J	Samples
SNJ54HC10W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403801DA SNJ54HC10W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC10, SN54HC10-SP, SN74HC10 :

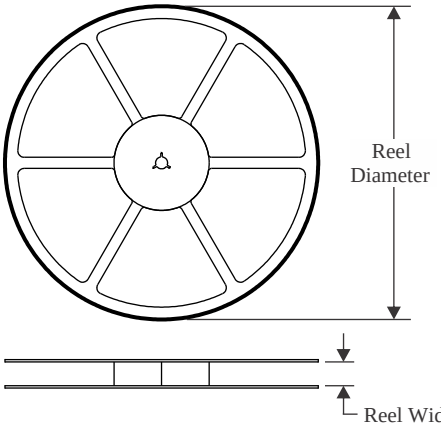
- Catalog : SN74HC10, SN54HC10
- Automotive : SN74HC10-Q1, SN74HC10-Q1
- Enhanced Product : SN74HC10-EP, SN74HC10-EP
- Military : SN54HC10
- Space : SN54HC10-SP

NOTE: Qualified Version Definitions:

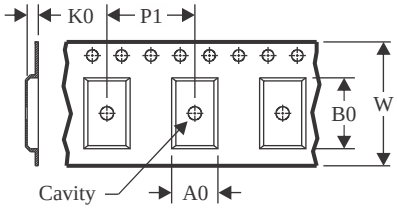
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

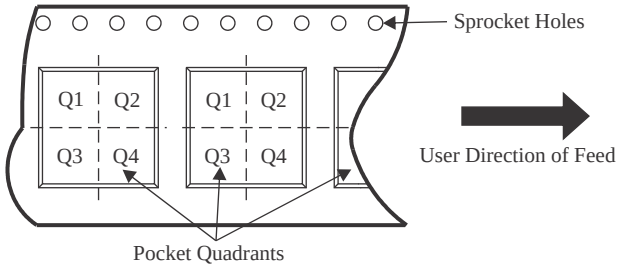


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

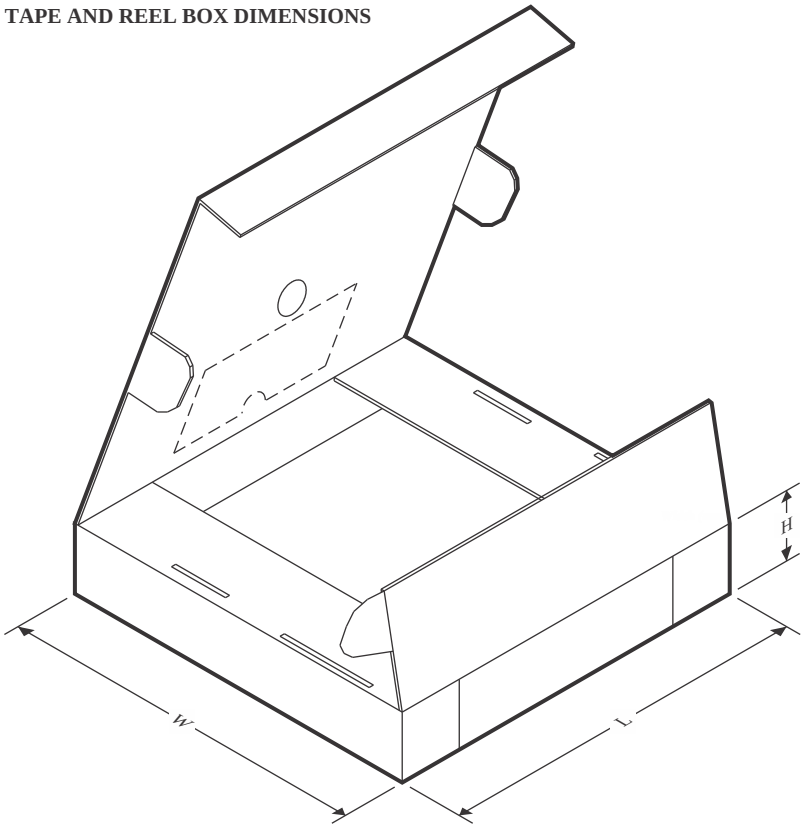
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC10DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC10DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HC10DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC10NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC10PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC10PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74HC10PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

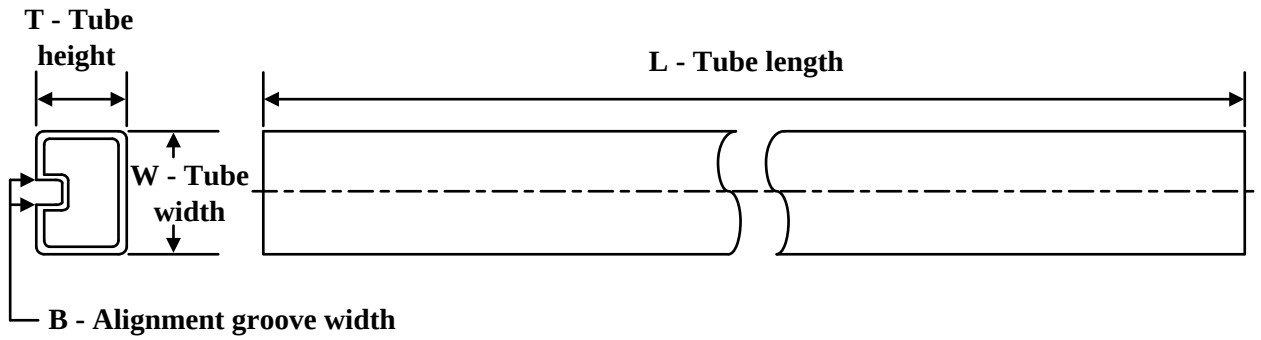
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC10DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC10DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HC10DT	SOIC	D	14	250	210.0	185.0	35.0
SN74HC10NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74HC10PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HC10PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74HC10PWT	TSSOP	PW	14	250	356.0	356.0	35.0

TUBE

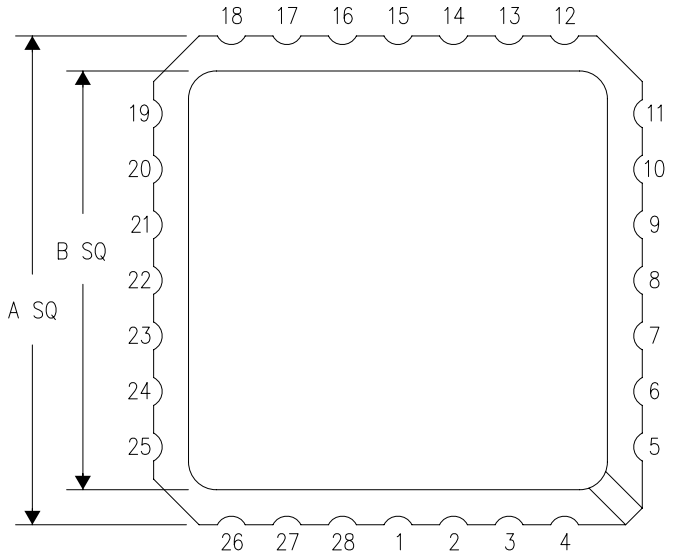


*All dimensions are nominal

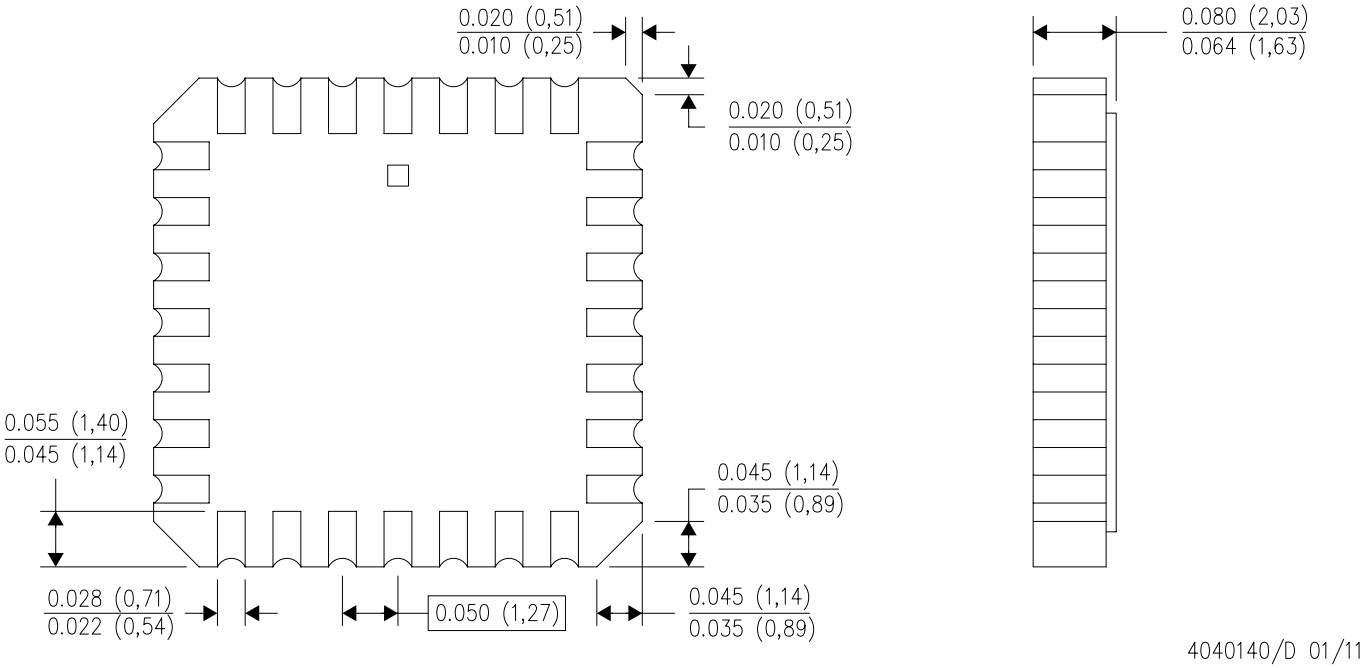
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
84038012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8403801DA	W	CFP	14	1	506.98	26.16	6220	NA
JM38510/65002B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/65002B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HC10D	D	SOIC	14	50	506.6	8	3940	4.32
SN74HC10DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74HC10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC10NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC10NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC10PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54HC10FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC10W	W	CFP	14	1	506.98	26.16	6220	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



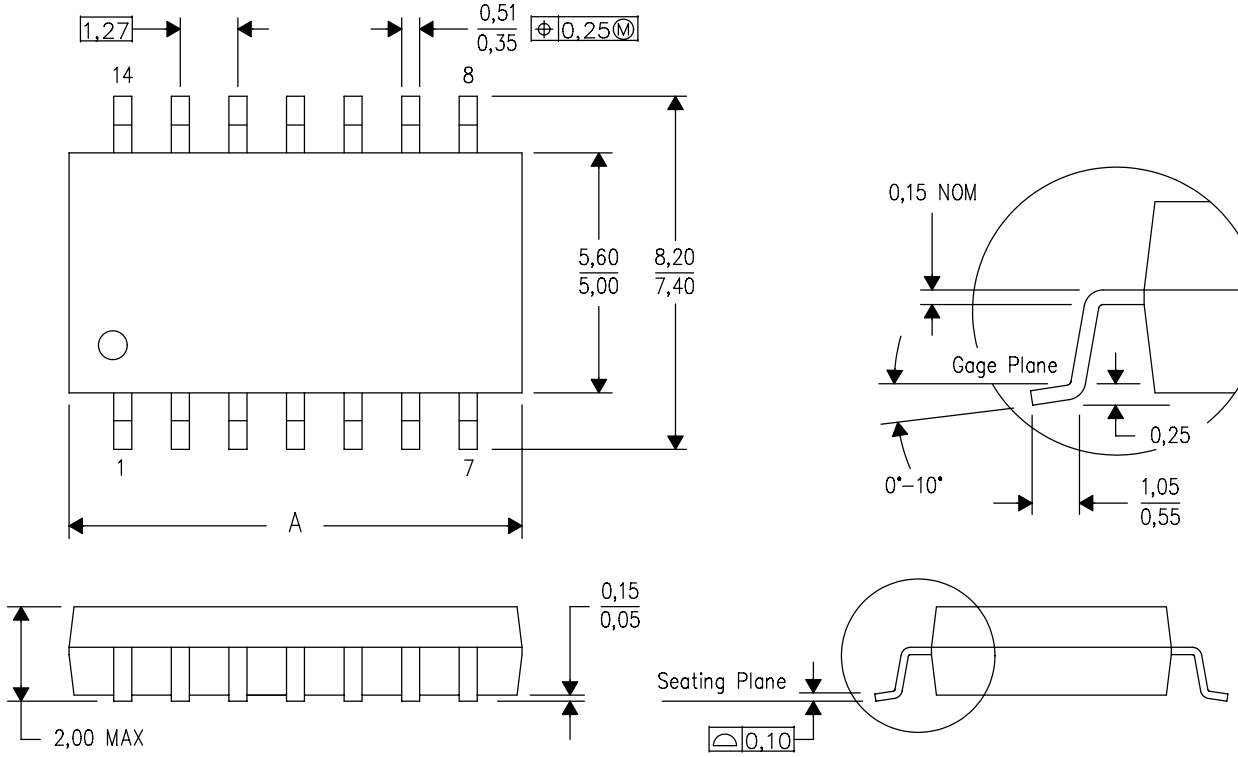
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

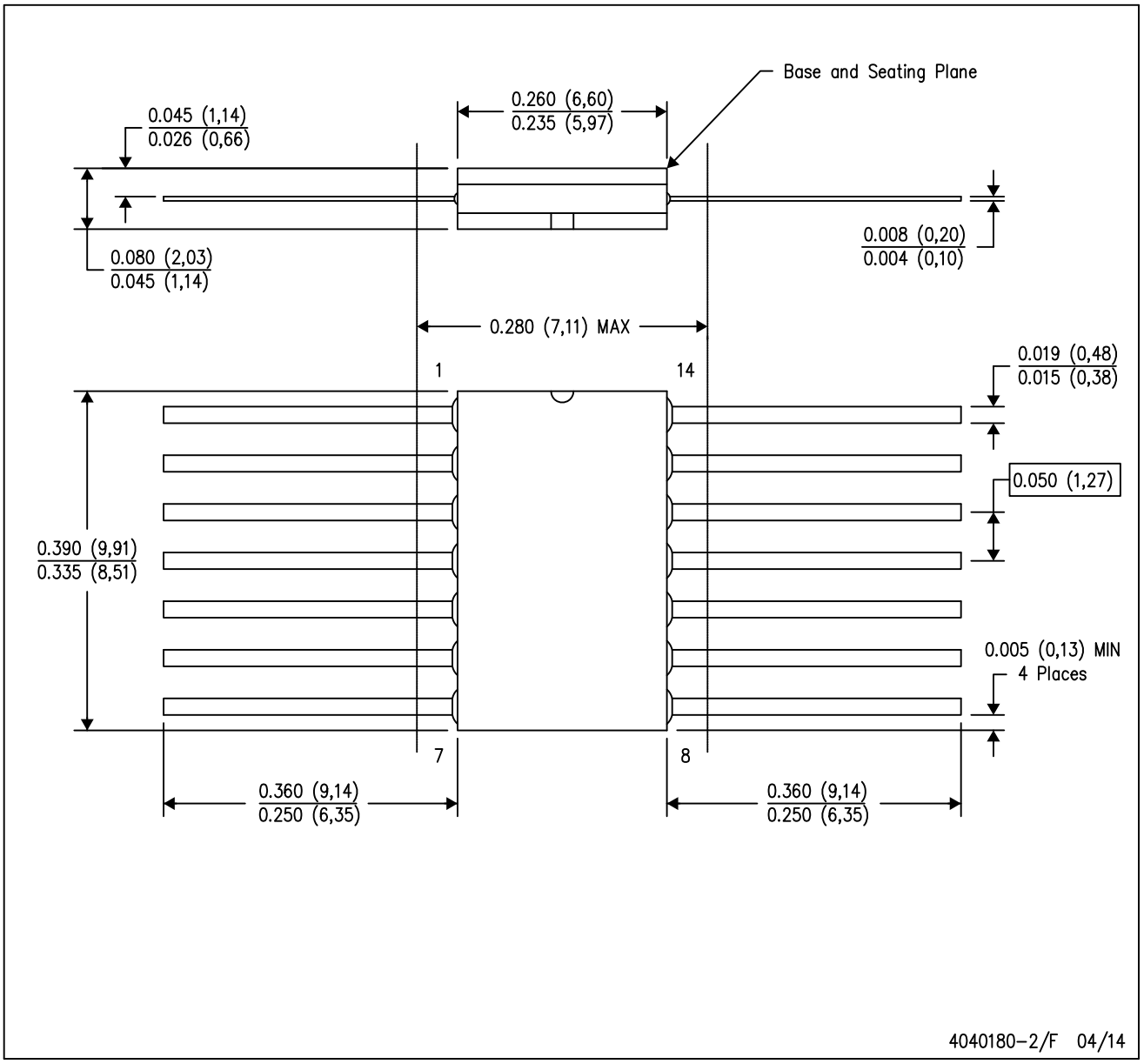


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

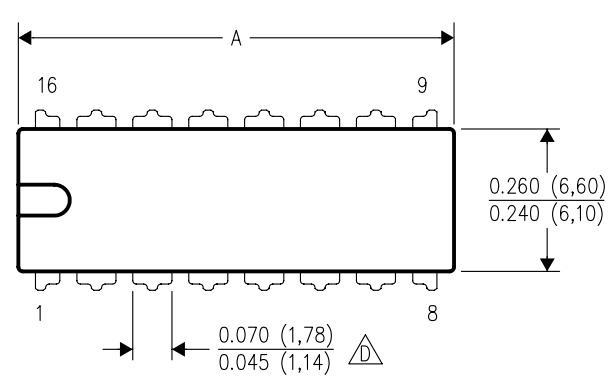


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

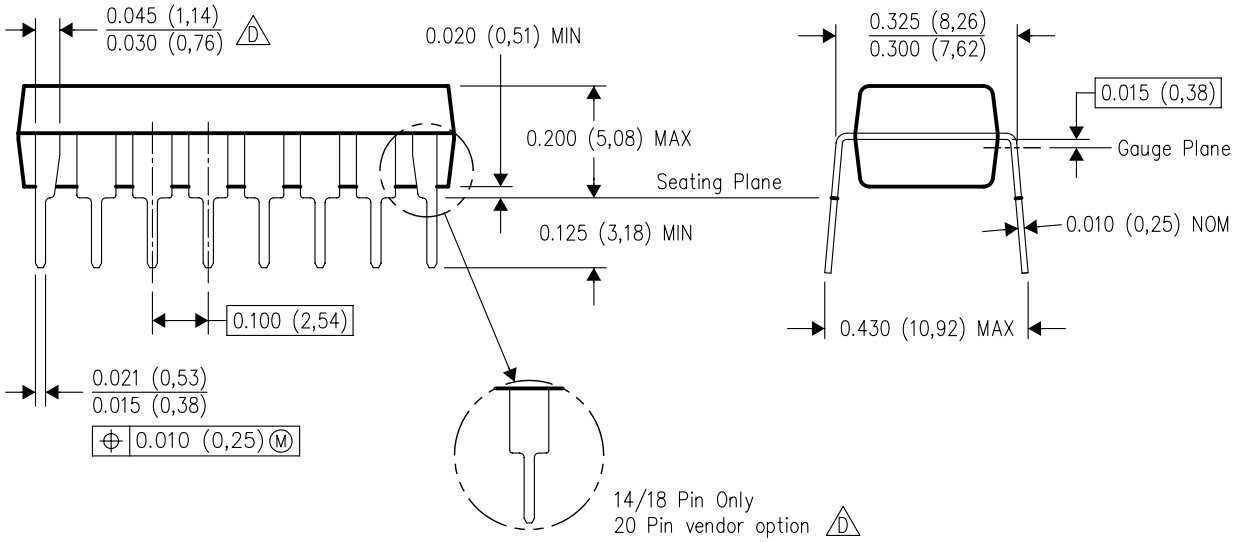
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



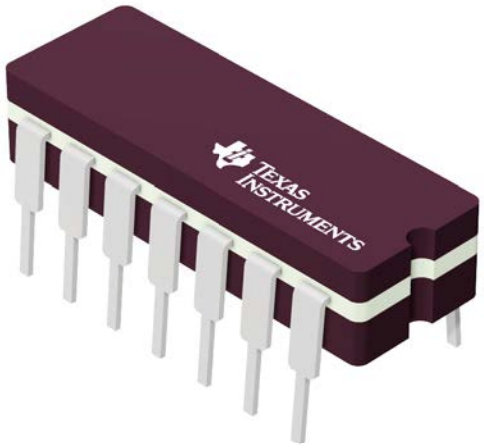
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

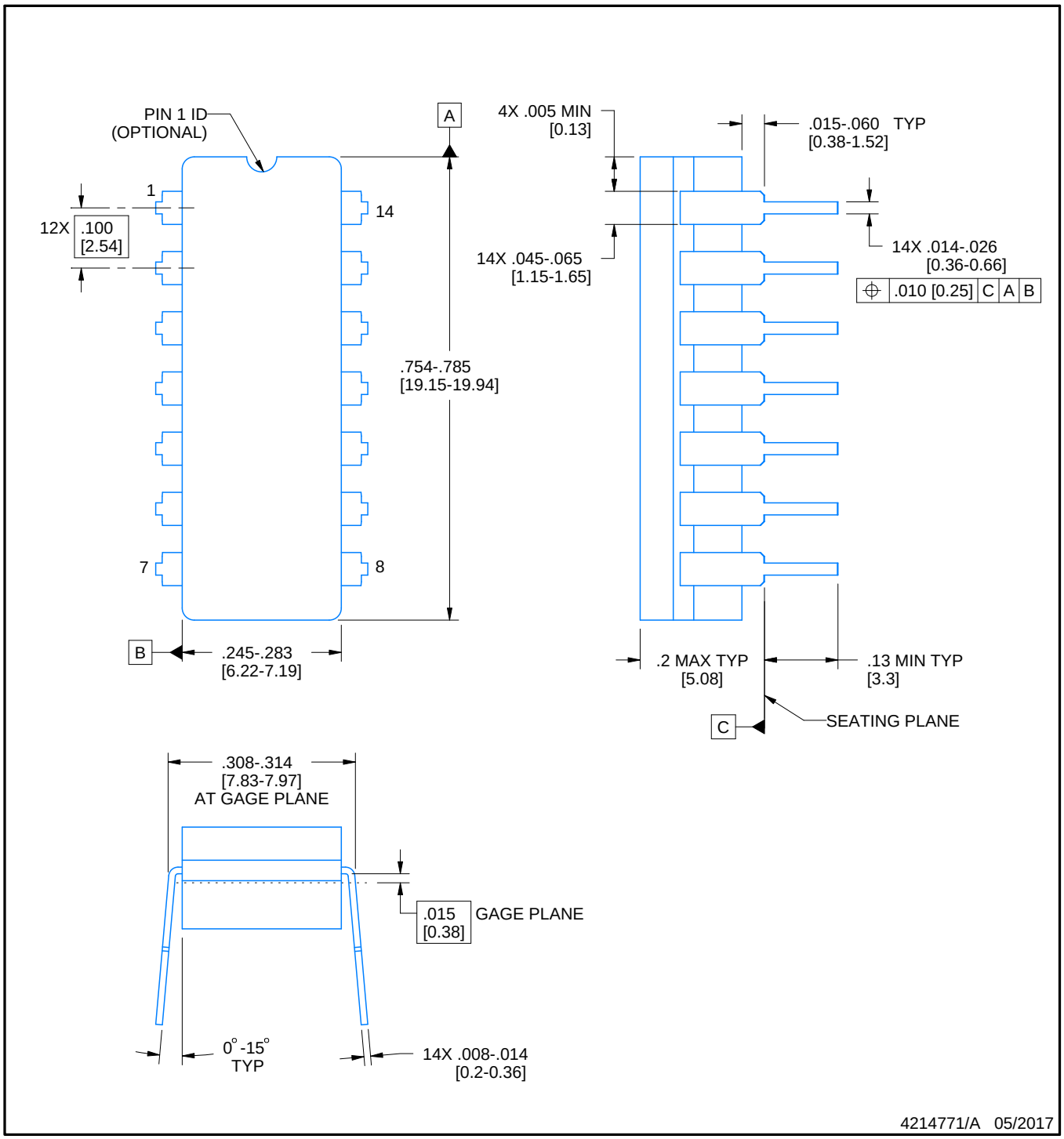
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

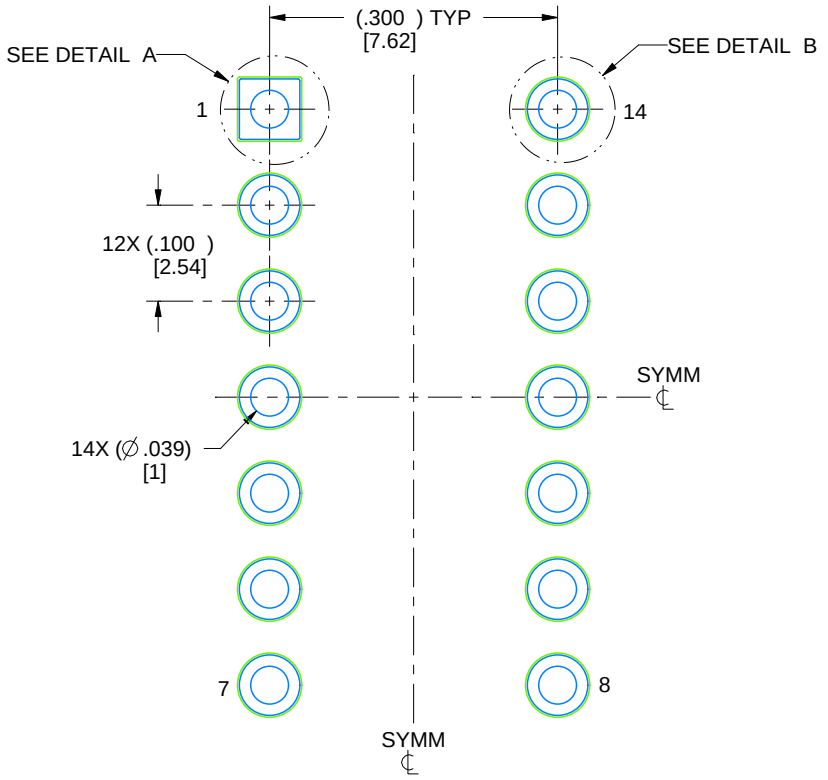
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

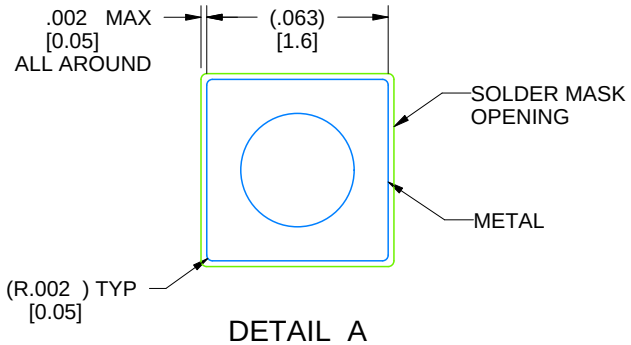
J0014A

CDIP - 5.08 mm max height

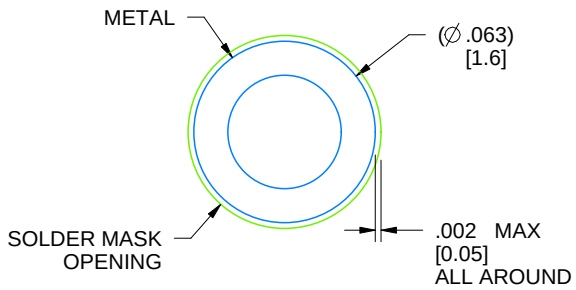
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



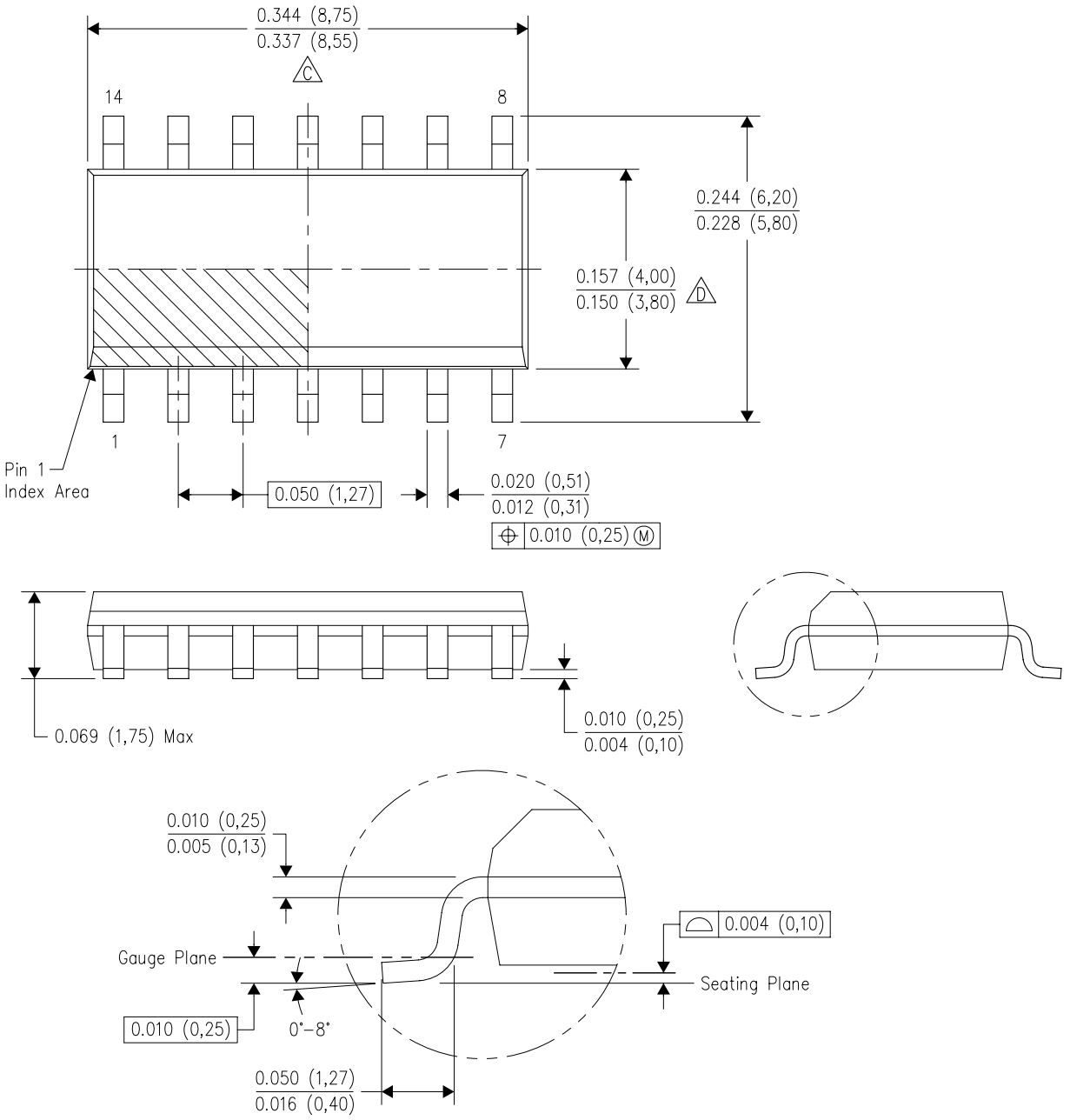
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

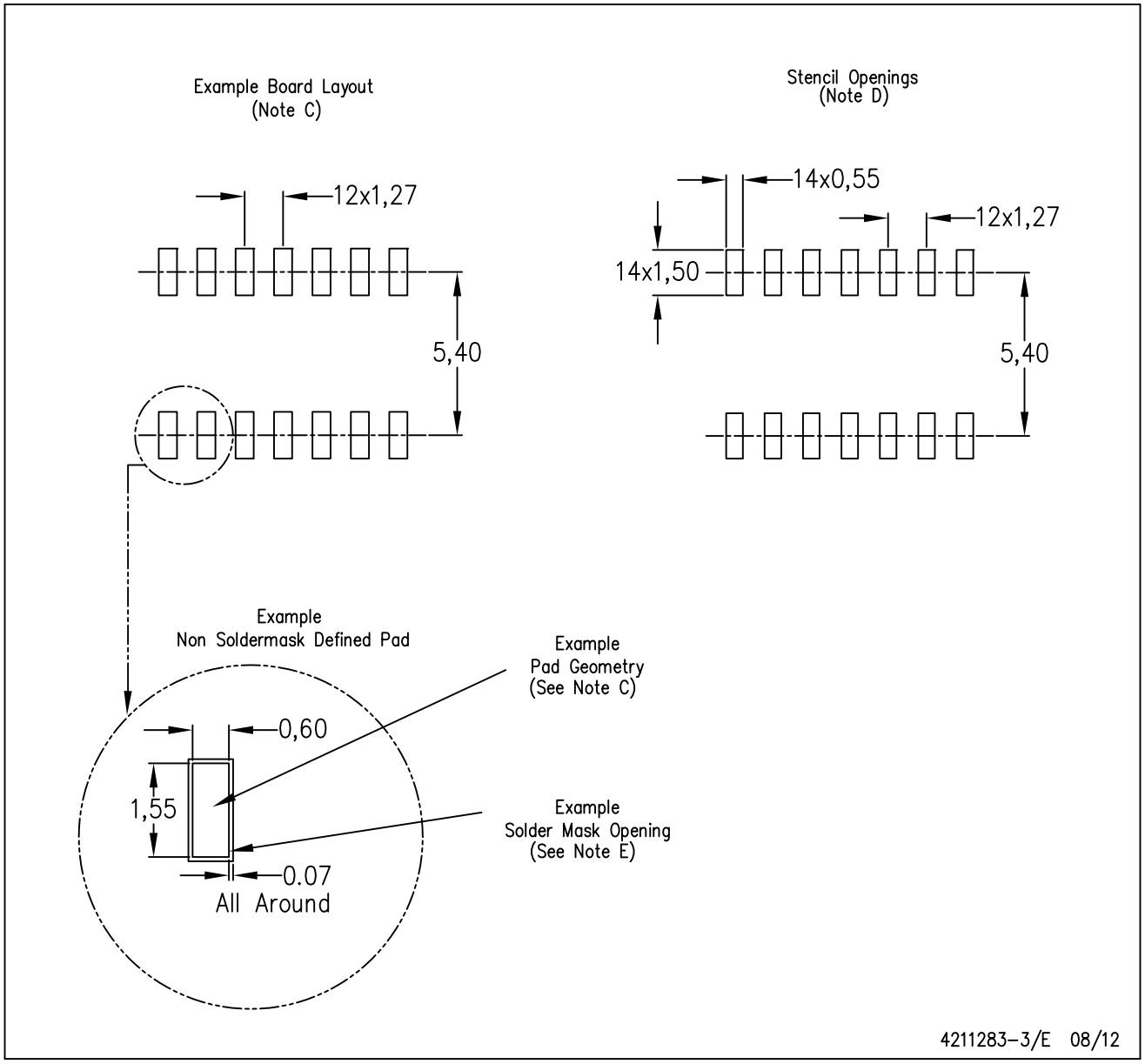
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

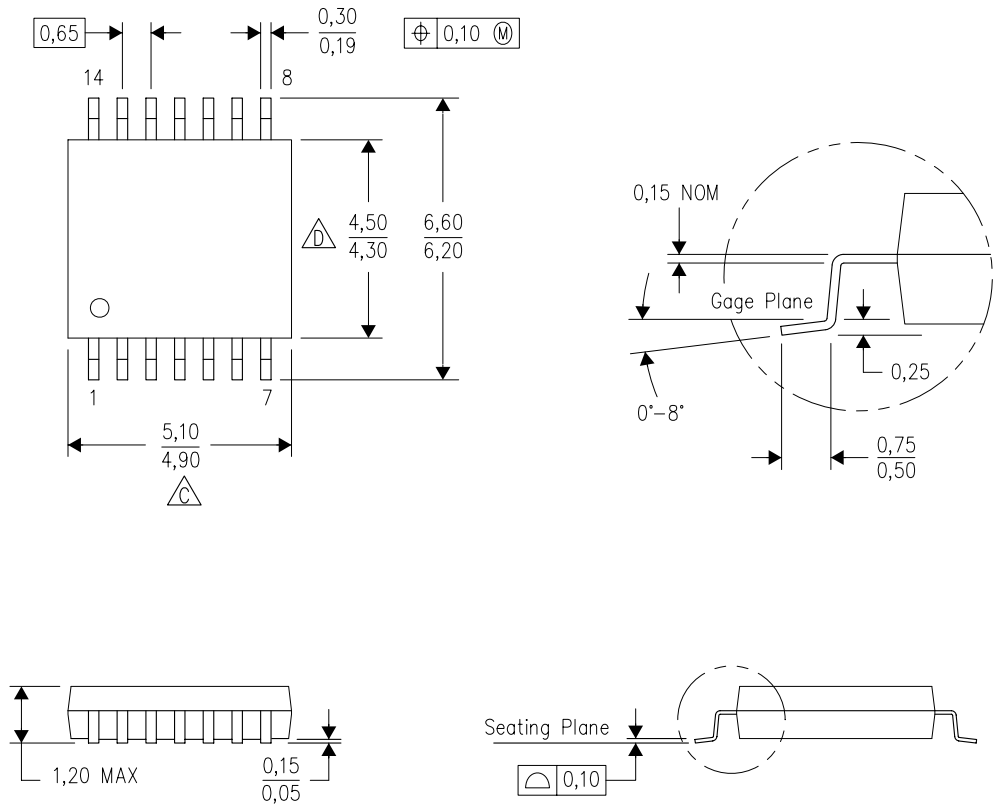
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

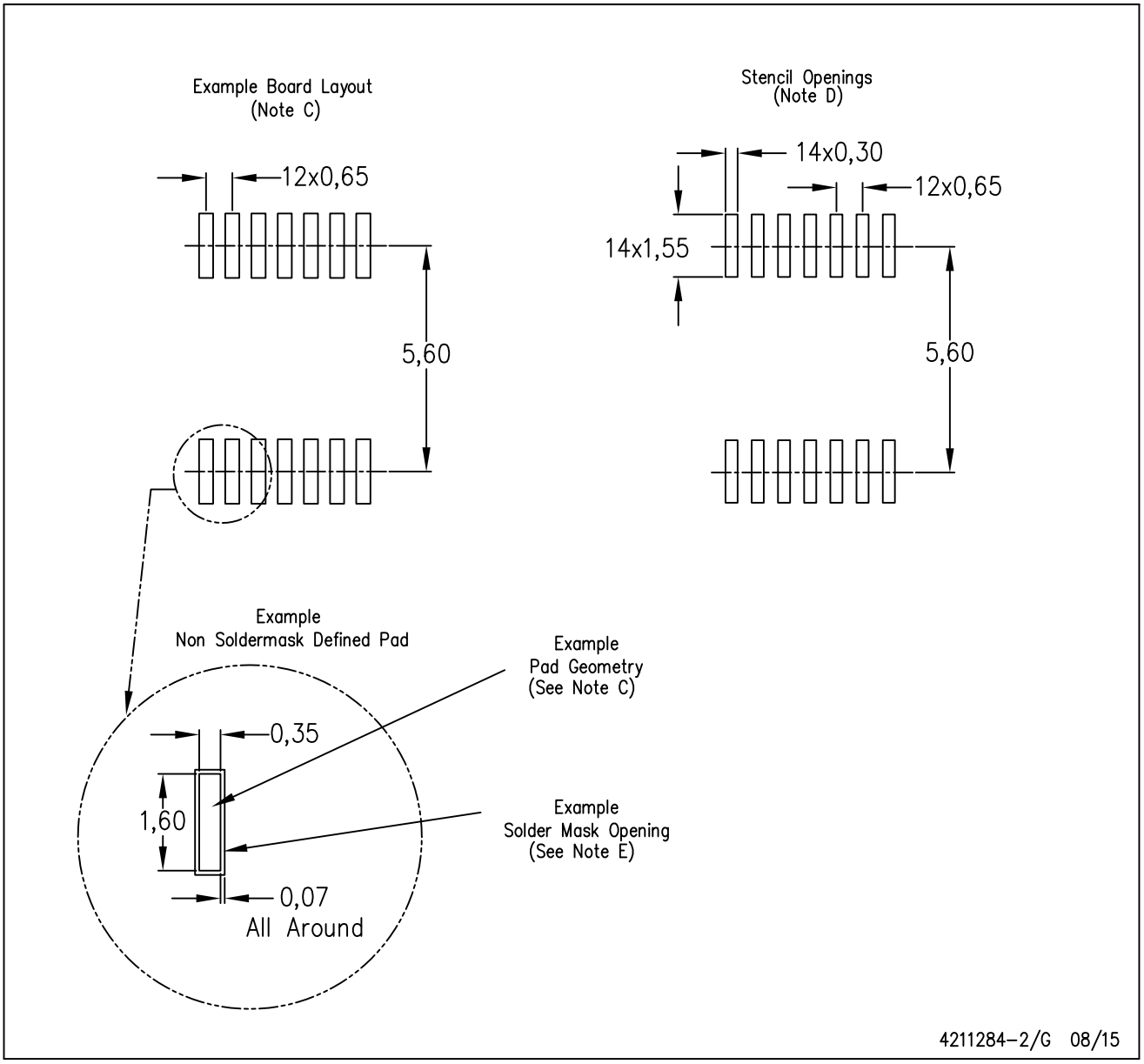
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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