

# Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

## 74FST3257

The onsemi 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

### Features

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: SOIC–16, TSSOP–16, QFN16
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

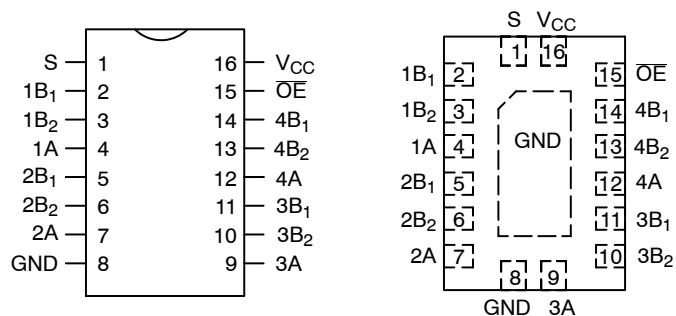


Figure 1. 16-Lead Pinout Diagrams

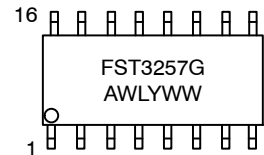
| S | OE | Function           |
|---|----|--------------------|
| X | H  | Disconnect         |
| L | L  | A = B <sub>1</sub> |
| H | L  | A = B <sub>2</sub> |

Figure 2. Truth Table

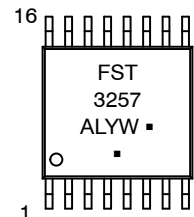
### MARKING DIAGRAMS



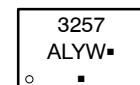
SOIC–16  
D SUFFIX  
CASE 751B



TSSOP–16  
DT SUFFIX  
CASE 948F



QFN16  
MN SUFFIX  
CASE 485AW



A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

### PIN NAMES

| Pin                                                               | Description        |
|-------------------------------------------------------------------|--------------------|
| OE <sub>1</sub> , OE <sub>2</sub>                                 | Bus Switch Enables |
| S <sub>0</sub> , S <sub>1</sub>                                   | Select Inputs      |
| A                                                                 | Bus A              |
| B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub> | Bus B              |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## 74FST3257

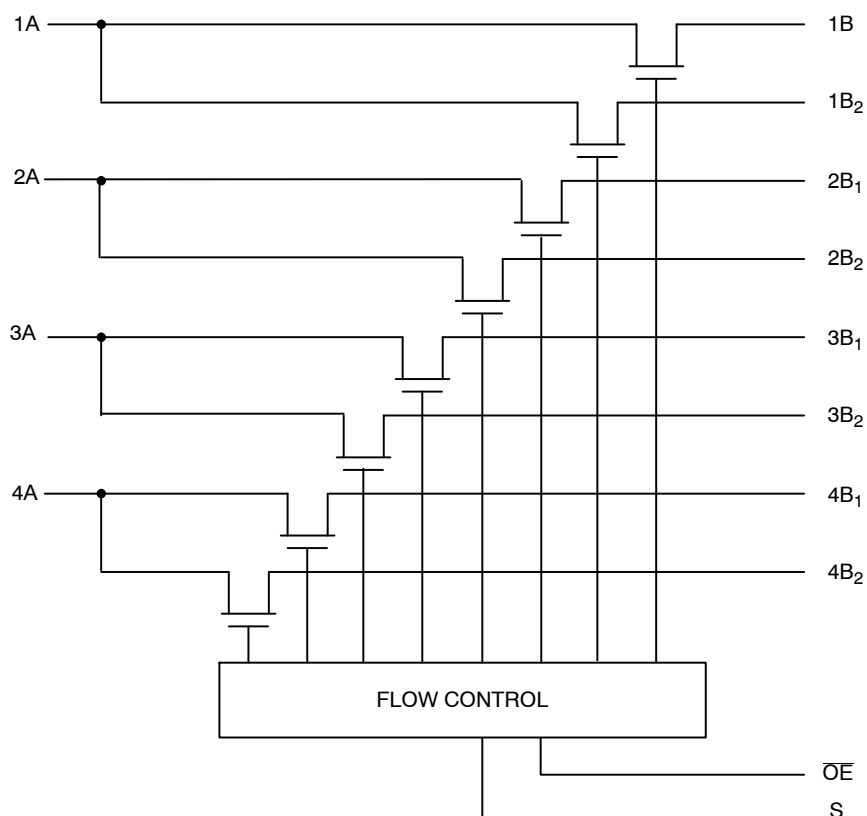


Figure 3. Logic Diagram

### ORDERING INFORMATION

| Device Order Number | Package               | Shipping <sup>†</sup>                                |
|---------------------|-----------------------|------------------------------------------------------|
| 74FST3257DR2G       | SOIC-16<br>(Pb-Free)  | 2500 Units / Tape & Reel                             |
| NLV74FST3257DR2G*   |                       |                                                      |
| 74FST3257DTR2G      | TSSOP-16<br>(Pb-Free) | 2500 Units / Tape & Reel                             |
| 74FST3257MNTWG      | QFN16<br>(Pb-Free)    | 3000 Units / Tape & Reel                             |
| 74FST3257MN2TWG     | QFN16<br>(Pb-Free)    | 3000 Units / Tape & Reel<br>(4mm pitch carrier tape) |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

**MAXIMUM RATINGS**

| Symbol        | Parameter                                                                                                     | Value                  | Units |
|---------------|---------------------------------------------------------------------------------------------------------------|------------------------|-------|
| $V_{CC}$      | DC Supply Voltage                                                                                             | -0.5 to +7.0           | V     |
| $V_I$         | DC Input Voltage                                                                                              | -0.5 to +7.0           | V     |
| $V_O$         | DC Output Voltage                                                                                             | -0.5 to +7.0           | V     |
| $I_{IK}$      | DC Input Diode Current<br>$V_I < GND$                                                                         | -50                    | mA    |
| $I_{OK}$      | DC Output Diode Current<br>$V_O < GND$                                                                        | -50                    | mA    |
| $I_O$         | DC Output Sink Current                                                                                        | 128                    | mA    |
| $I_{CC}$      | DC Supply Current per Supply Pin                                                                              | $\pm 100$              | mA    |
| $I_{GND}$     | DC Ground Current per Ground Pin                                                                              | $\pm 100$              | mA    |
| $T_{STG}$     | Storage Temperature Range                                                                                     | -65 to +150            | °C    |
| $T_L$         | Lead Temperature, 1 mm from Case for 10 Seconds                                                               | 260                    | °C    |
| $T_J$         | Junction Temperature Under Bias                                                                               | +150                   | °C    |
| $\theta_{JA}$ | Thermal Resistance<br>SOIC<br>TSSOP<br>QFN                                                                    | 125<br>170<br>N/A      | °C/W  |
| MSL           | Moisture Sensitivity                                                                                          | Level 1                |       |
| $F_R$         | Flammability Rating<br>Oxygen Index: 28 to 34                                                                 | UL 94 V-0 @ 0.125 in   |       |
| $V_{ESD}$     | ESD Withstand Voltage<br>Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | > 2000<br>> 200<br>N/A | V     |
| $I_{Latchup}$ | Latchup Performance<br>Above $V_{CC}$ and Below GND at 85°C (Note 4)                                          | $\pm 500$              | mA    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol              | Parameter                                        | Min | Max     | Units |
|---------------------|--------------------------------------------------|-----|---------|-------|
| $V_{CC}$            | Supply Voltage<br>Operating, Data Retention Only | 4.0 | 5.5     | V     |
| $V_I$               | Input Voltage (Note 5)                           | 0   | 5.5     | V     |
| $V_O$               | Output Voltage (HIGH or LOW State)               | 0   | 5.5     | V     |
| $T_A$               | Operating Free-Air Temperature                   | -40 | +85     | °C    |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate<br>Switch I/O | 0   | DC<br>5 | ns/V  |

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

## DC ELECTRICAL CHARACTERISTICS

| Symbol           | Parameter                             | Conditions                                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> = -40°C to +85°C |      |      | Units |
|------------------|---------------------------------------|----------------------------------------------------------------|------------------------|---------------------------------|------|------|-------|
|                  |                                       |                                                                |                        | Min                             | Typ* | Max  |       |
| V <sub>IK</sub>  | Clamp Diode Voltage                   | I <sub>IN</sub> = -18 mA                                       | 4.5                    |                                 |      | -1.2 | V     |
| V <sub>IH</sub>  | High-Level Input Voltage              |                                                                | 4.0 to 5.5             | 2.0                             |      |      | V     |
| V <sub>IL</sub>  | Low-Level Input Voltage               |                                                                | 4.0 to 5.5             |                                 |      | 0.8  | V     |
| I <sub>I</sub>   | Input Leakage Current                 | 0 ≤ V <sub>IN</sub> ≤ 5.5 V                                    | 5.5                    |                                 |      | ±1.0 | μA    |
| I <sub>OZ</sub>  | Off-State Leakage Current             | 0 ≤ A, B ≤ V <sub>CC</sub>                                     | 5.5                    |                                 |      | ±1.0 | μA    |
| R <sub>ON</sub>  | Switch On Resistance (Note 6)         | V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA                 | 4.5                    |                                 | 4    | 7    | Ω     |
|                  |                                       | V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA                 | 4.5                    |                                 | 4    | 7    |       |
|                  |                                       | V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA               | 4.5                    |                                 | 8    | 15   |       |
|                  |                                       | V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA               | 4.0                    |                                 | 11   | 20   |       |
| I <sub>CC</sub>  | Quiescent Supply Current              | V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0 | 5.5                    |                                 |      | 3    | μA    |
| ΔI <sub>CC</sub> | Increase In I <sub>CC</sub> per Input | One input at 3.4 V,<br>Other inputs at V <sub>CC</sub> or GND  | 5.5                    |                                 |      | 2.5  | mA    |

\*Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC ELECTRICAL CHARACTERISTICS

| Symbol                                 | Parameter                                        | Conditions                                 | T <sub>A</sub> = -40°C to +85°C<br>C <sub>L</sub> = 50 pF, R <sub>U</sub> = R <sub>D</sub> = 500 Ω |      |                         |      | Units |
|----------------------------------------|--------------------------------------------------|--------------------------------------------|----------------------------------------------------------------------------------------------------|------|-------------------------|------|-------|
|                                        |                                                  |                                            | V <sub>CC</sub> = 4.5-5.5 V                                                                        |      | V <sub>CC</sub> = 4.0 V |      |       |
|                                        |                                                  |                                            | Min                                                                                                | Max  | Min                     | Max  |       |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Prop Delay Bus to Bus (Note 7)                   | V <sub>I</sub> = OPEN                      |                                                                                                    | 0.25 |                         | 0.25 | ns    |
|                                        | Prop Delay, Select to Bus A                      |                                            | 1.0                                                                                                | 4.7  |                         | 5.2  |       |
| t <sub>PZH</sub> ,<br>t <sub>PZL</sub> | Output Enable Time, Select to Bus B              | V <sub>I</sub> = 7 V for t <sub>pZL</sub>  | 1.0                                                                                                | 5.2  |                         | 5.7  | ns    |
|                                        | Output Enable Time, I <sub>OE</sub> to Bus A, B  | V <sub>I</sub> = OPEN for t <sub>pZH</sub> | 1.0                                                                                                | 5.1  |                         | 5.6  |       |
| t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> | Output Disable Time, Select to Bus B             | V <sub>I</sub> = 7 V for t <sub>pLZ</sub>  | 1.0                                                                                                | 5.2  |                         | 5.5  | ns    |
|                                        | Output Disable Time, I <sub>OE</sub> to Bus A, B | V <sub>I</sub> = OPEN for t <sub>pHZ</sub> | 1.0                                                                                                | 5.5  |                         | 5.5  |       |

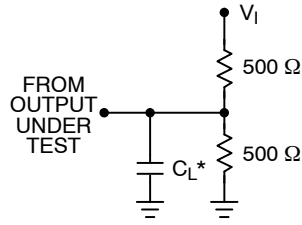
7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## CAPACITANCE (Note 8)

| Symbol           | Parameter                       | Conditions                                       | Typ | Max | Units |
|------------------|---------------------------------|--------------------------------------------------|-----|-----|-------|
| C <sub>IN</sub>  | Control Pin Input Capacitance   | V <sub>CC</sub> = 5.0 V                          | 3   |     | pF    |
| C <sub>I/O</sub> | A Port Input/Output Capacitance | V <sub>CC</sub> , $\overline{\text{OE}}$ = 5.0 V | 7   |     | pF    |
| C <sub>I/O</sub> | B Port Input/Output Capacitance | V <sub>CC</sub> , $\overline{\text{OE}}$ = 5.0 V | 5   |     | pF    |

8. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

# AC Loading and Waveforms



## NOTES:

1. Input driven by 50  $\Omega$  source terminated in 50  $\Omega$ .
  2.  $C_L$  includes load and stray capacitance.
- \* $C_L = 50$  pF

Figure 4. AC Test Circuit

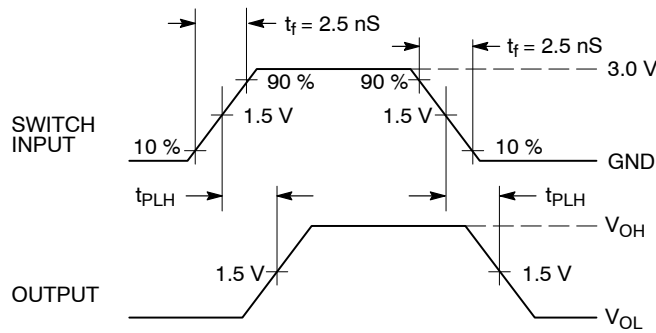


Figure 5. Propagation Delays

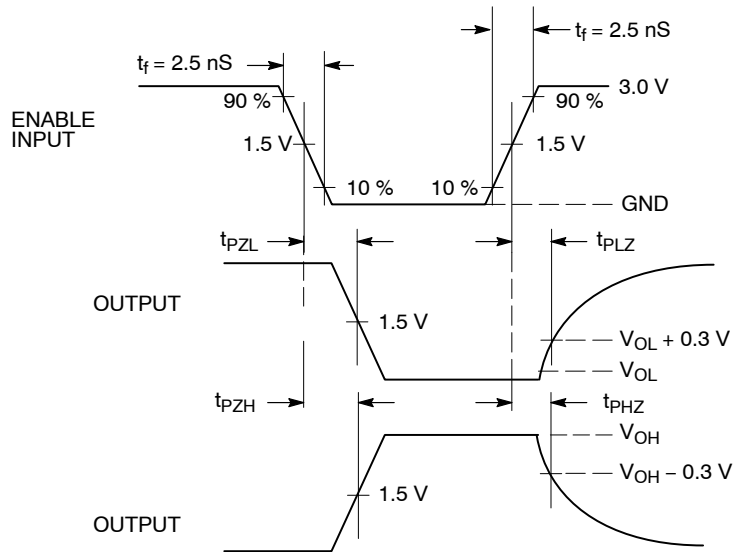


Figure 6. Enable/Disable Delays

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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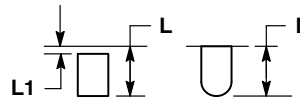
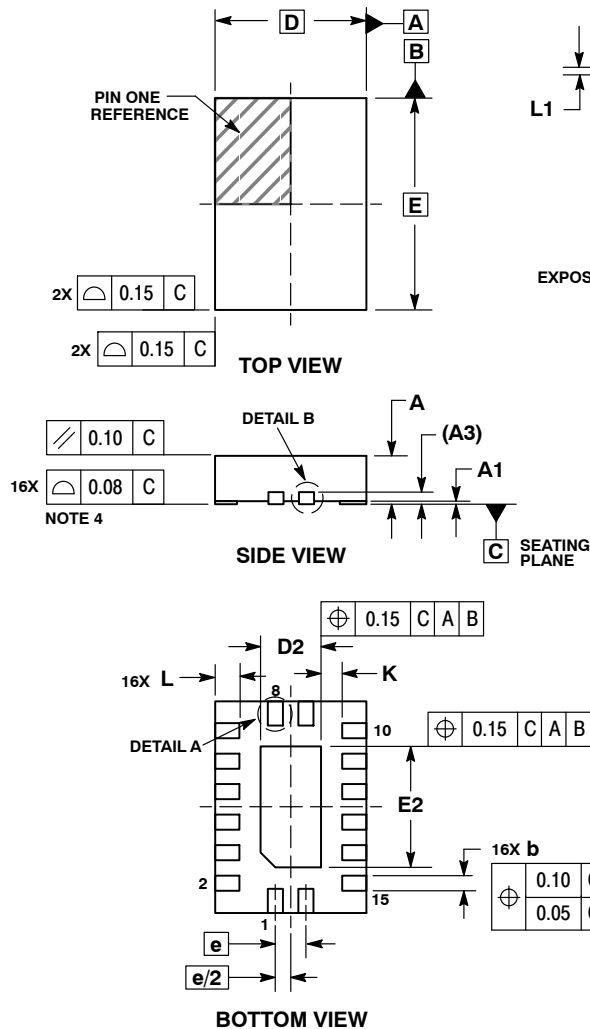
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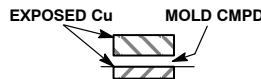
SCALE 2:1

**QFN16, 2.5x3.5, 0.5P**  
CASE 485AW-01  
ISSUE O

DATE 11 DEC 2008



**DETAIL A**  
ALTERNATE TERMINAL  
CONSTRUCTIONS



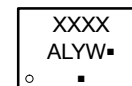
**DETAIL B**  
ALTERNATE  
CONSTRUCTIONS

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.50 BSC    |      |
| D2  | 0.85        | 1.15 |
| E   | 3.50 BSC    |      |
| E2  | 1.85        | 2.15 |
| e   | 0.50 BSC    |      |
| K   | 0.20        | ---  |
| L   | 0.35        | 0.45 |
| L1  | ---         | 0.15 |

### GENERIC MARKING DIAGRAM\*

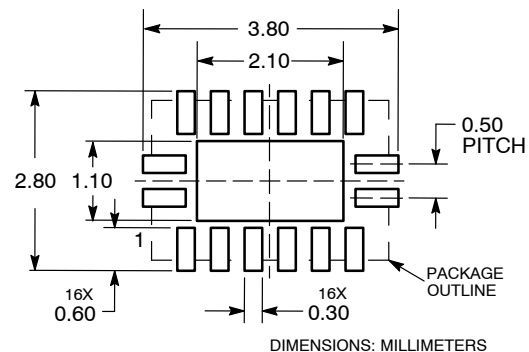


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                             |                                                                                                                                                                                  |
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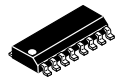
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

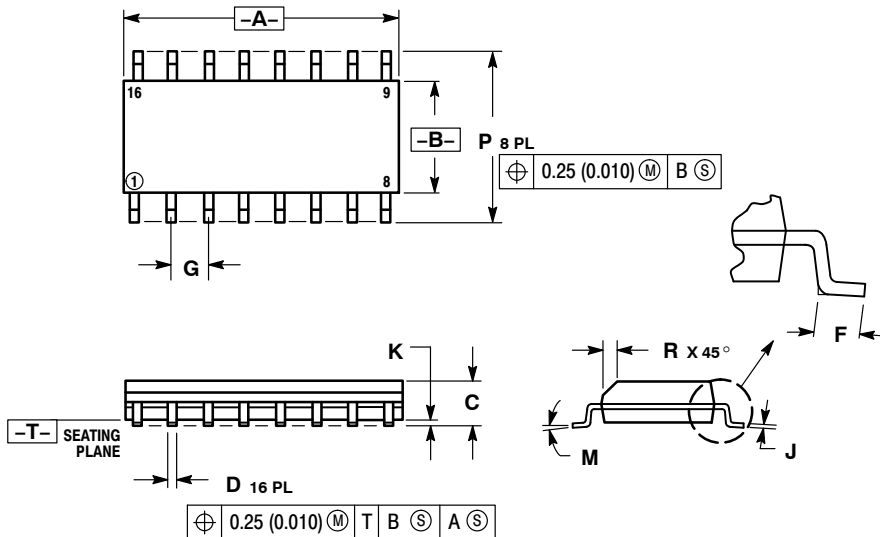
ON



SCALE 1:1

### SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



#### NOTES:

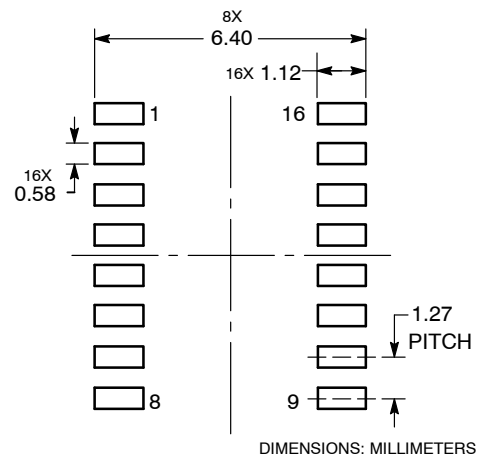
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| E   | 0.40        | 1.25  | 0.016     | 0.049 |
| F   | 1.27 BSC    |       | 0.050 BSC |       |
| G   | 0.19        | 0.25  | 0.008     | 0.009 |
| H   | 0.10        | 0.25  | 0.004     | 0.009 |
| I   | 0°          | 7°    | 0°        | 7°    |
| J   | 5.80        | 6.20  | 0.229     | 0.244 |
| K   | 0.25        | 0.50  | 0.010     | 0.019 |

|                   |                   |                          |                          |
|-------------------|-------------------|--------------------------|--------------------------|
| STYLE 1:          | STYLE 2:          | STYLE 3:                 | STYLE 4:                 |
| PIN 1. COLLECTOR  | PIN 1. CATHODE    | PIN 1. COLLECTOR, DYE #1 | PIN 1. COLLECTOR, DYE #1 |
| 2. BASE           | 2. ANODE          | 2. BASE, #1              | 2. COLLECTOR, #1         |
| 3. EMITTER        | 3. NO CONNECTION  | 3. EMITTER, #1           | 3. COLLECTOR, #2         |
| 4. NO CONNECTION  | 4. CATHODE        | 4. COLLECTOR, #1         | 4. COLLECTOR, #2         |
| 5. EMITTER        | 5. CATHODE        | 5. COLLECTOR, #2         | 5. COLLECTOR, #3         |
| 6. BASE           | 6. NO CONNECTION  | 6. BASE, #2              | 6. COLLECTOR, #3         |
| 7. COLLECTOR      | 7. ANODE          | 7. EMITTER, #2           | 7. COLLECTOR, #4         |
| 8. COLLECTOR      | 8. CATHODE        | 8. COLLECTOR, #2         | 8. COLLECTOR, #4         |
| 9. BASE           | 9. CATHODE        | 9. COLLECTOR, #3         | 9. BASE, #4              |
| 10. EMITTER       | 10. ANODE         | 10. BASE, #3             | 10. EMITTER, #4          |
| 11. NO CONNECTION | 11. NO CONNECTION | 11. EMITTER, #3          | 11. BASE, #3             |
| 12. EMITTER       | 12. CATHODE       | 12. COLLECTOR, #3        | 12. EMITTER, #3          |
| 13. BASE          | 13. CATHODE       | 13. COLLECTOR, #4        | 13. BASE, #2             |
| 14. COLLECTOR     | 14. NO CONNECTION | 14. BASE, #4             | 14. EMITTER, #2          |
| 15. EMITTER       | 15. ANODE         | 15. EMITTER, #4          | 15. BASE, #1             |
| 16. COLLECTOR     | 16. CATHODE       | 16. COLLECTOR, #4        | 16. EMITTER, #1          |

|                      |                |                           |
|----------------------|----------------|---------------------------|
| STYLE 5:             | STYLE 6:       | STYLE 7:                  |
| PIN 1. DRAIN, DYE #1 | PIN 1. CATHODE | PIN 1. SOURCE N-CH        |
| 2. DRAIN, #1         | 2. CATHODE     | 2. COMMON DRAIN (OUTPUT)  |
| 3. DRAIN, #2         | 3. CATHODE     | 3. COMMON DRAIN (OUTPUT)  |
| 4. DRAIN, #2         | 4. CATHODE     | 4. GATE P-CH              |
| 5. DRAIN, #3         | 5. CATHODE     | 5. COMMON DRAIN (OUTPUT)  |
| 6. DRAIN, #3         | 6. CATHODE     | 6. COMMON DRAIN (OUTPUT)  |
| 7. DRAIN, #4         | 7. CATHODE     | 7. COMMON DRAIN (OUTPUT)  |
| 8. DRAIN, #4         | 8. CATHODE     | 8. SOURCE P-CH            |
| 9. GATE, #4          | 9. ANODE       | 9. SOURCE P-CH            |
| 10. SOURCE, #4       | 10. ANODE      | 10. COMMON DRAIN (OUTPUT) |
| 11. GATE, #3         | 11. ANODE      | 11. COMMON DRAIN (OUTPUT) |
| 12. SOURCE, #3       | 12. ANODE      | 12. COMMON DRAIN (OUTPUT) |
| 13. GATE, #2         | 13. ANODE      | 13. GATE N-CH             |
| 14. SOURCE, #2       | 14. ANODE      | 14. COMMON DRAIN (OUTPUT) |
| 15. GATE, #1         | 15. ANODE      | 15. COMMON DRAIN (OUTPUT) |
| 16. SOURCE, #1       | 16. ANODE      | 16. SOURCE N-CH           |

#### SOLDERING FOOTPRINT



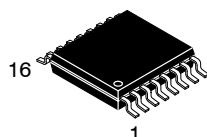
DIMENSIONS: MILLIMETERS

|                  |             |                                                                                                                                                                                     |
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

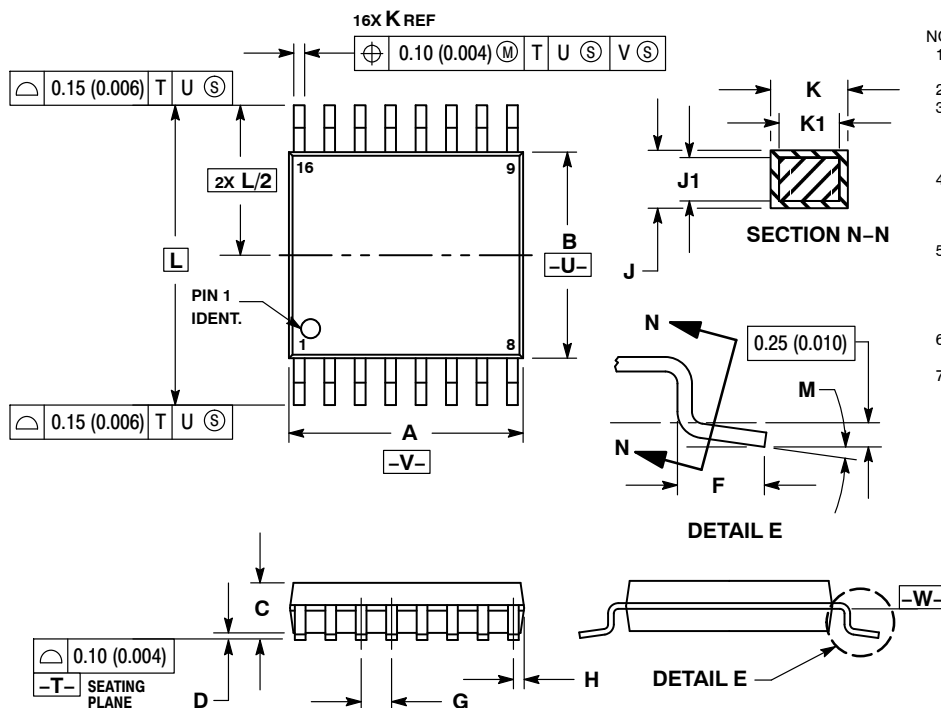
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SCALE 2:1

## TSSOP-16 CASE 948F-01 ISSUE B

DATE 19 OCT 2006

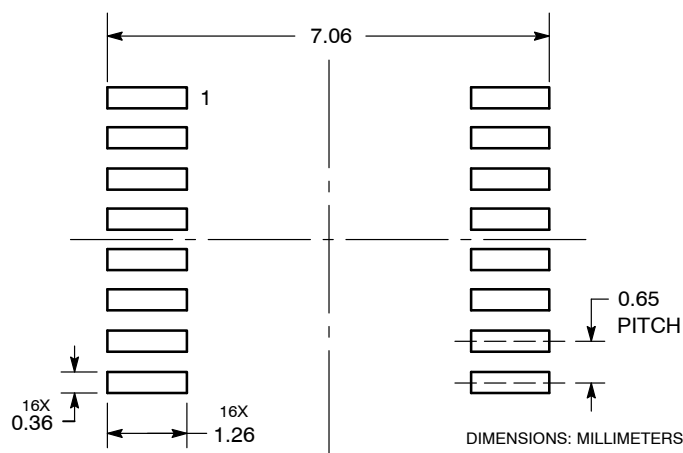


### NOTES:

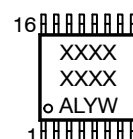
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

|                  |             |                                                                                                                                                                                  |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | TSSOP-16    | PAGE 1 OF 1                                                                                                                                                                      |

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